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10/724,903	12/01/2003	Grit Schwalbe	P2001,0368	3287

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EXAMINER	
COLEMAN, WILLIAM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,903	SCHWALBE ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~1203~~ 01/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-16 and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by An, U.S. Patent 5,624,862.

3. An discloses a semiconductor process as claimed. See **FIGS. 1-4F**, where An teaches the claimed limitations.

4. Pertaining to claim 1, An teaches a method for providing bitline contacts in a memory cell array, which comprises:

disposing a plurality of bitlines in a first direction;

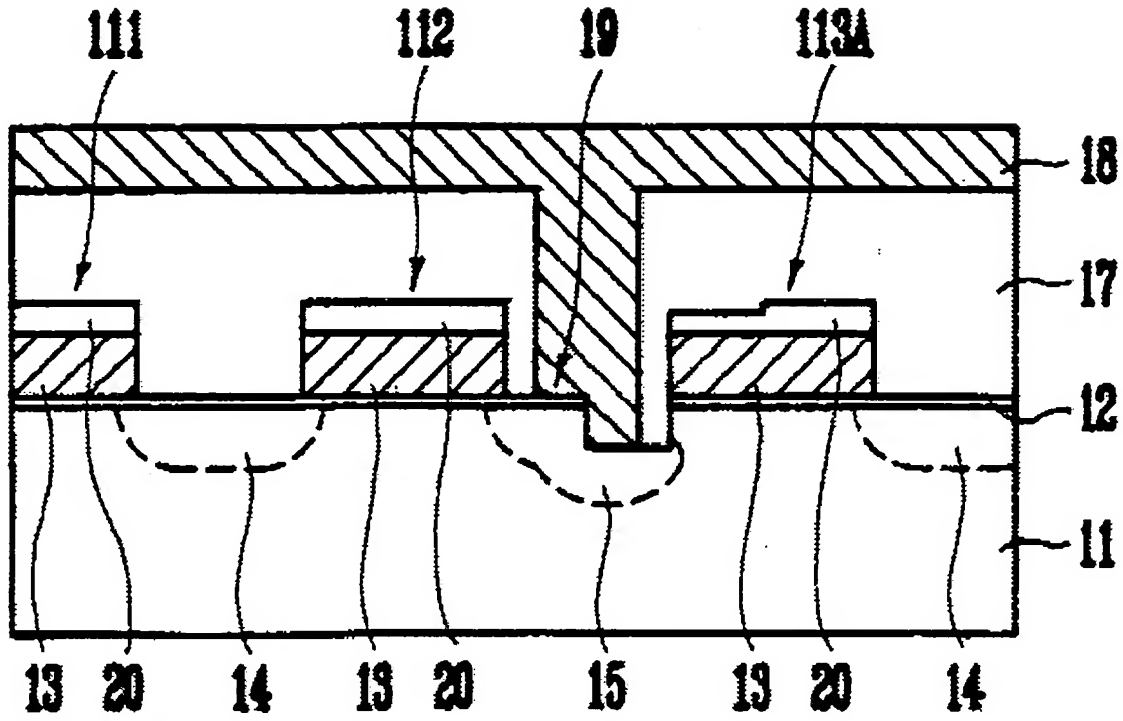
covering the bitlines with an isolating layer;

disposing a plurality of wordlines in a second direction crossing the first direction above the bitlines;

disposing memory cells where the bitlines and wordlines cross one another;

removing the isolating layer from the bitlines at portions not covered by the wordlines with areas between the bitlines remaining unaffected; and

providing an electrical conductive material on exposed portions of the bitlines.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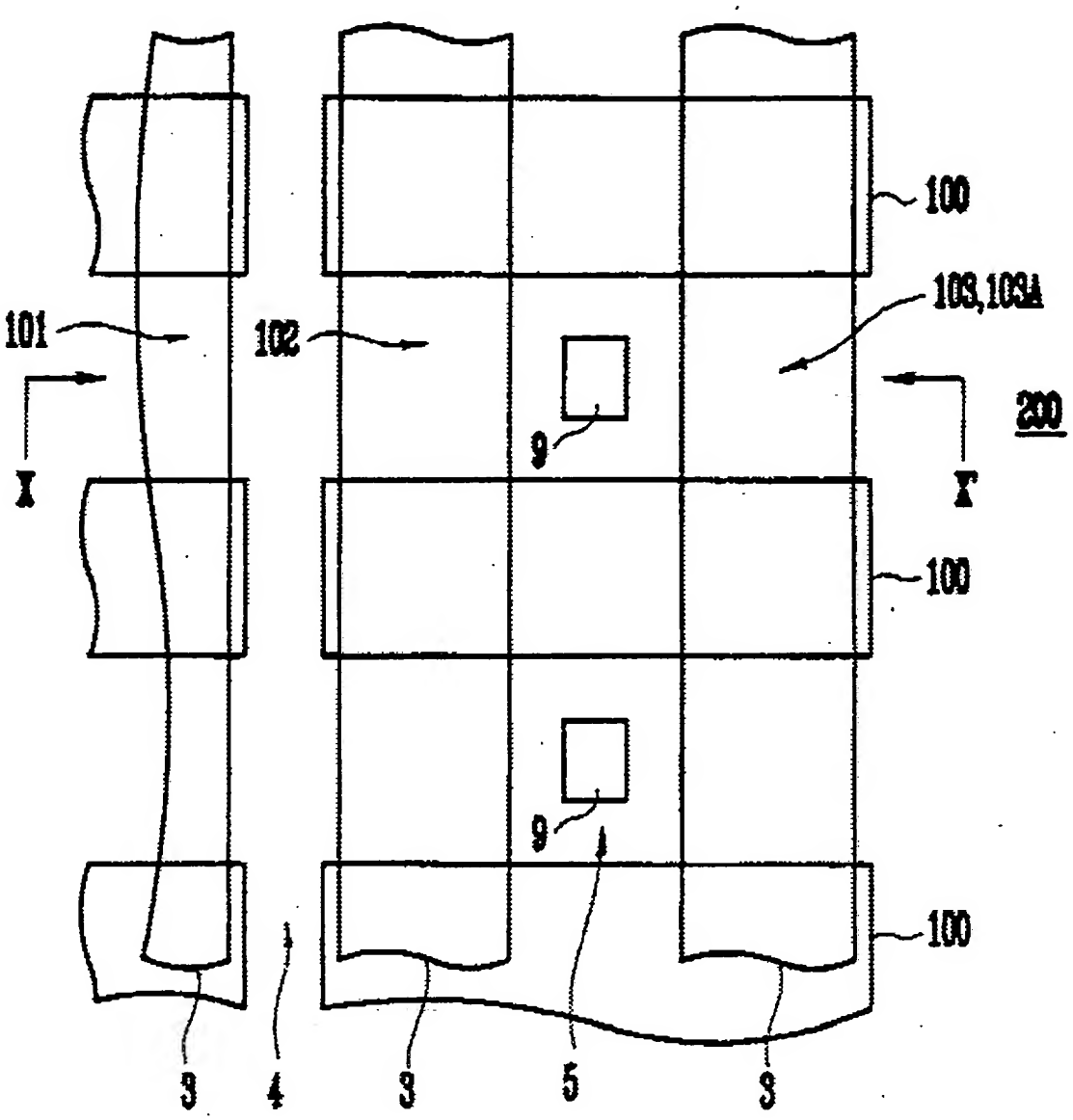

5. Pertaining to claim 2, An teaches the method according to claim 1, which further comprises carrying out the step of removing the isolating layer from the bitlines by:

depositing a photoresist material;

patterning the photoresist material using a mask having a stripe pattern; and;

selectively etching the isolating layer with respect to the wordlines.

6. Pertaining to claim 3, An teaches the method according to claim 2, which further comprises providing the mask having the stripe pattern as the bitline **12** mask by which the bitlines have been defined.

7. Pertaining to claim 9, An teaches the method according to claim 2, which further comprises carrying out the bitline disposing step by disposing the bitlines with the mask having the stripe pattern.

8. Pertaining to claim 5, An teaches a method for providing bitline contacts in a memory cell array, which comprises:

disposing a plurality of bitlines in a first direction on a substrate;

disposing a plurality of wordlines in a second direction crossing the first direction above the bitlines on the substrate;

disposing memory cells where the bitlines and wordlines cross one another, the memory cells forming a memory cell array;

covering the bitlines with a first isolating layer;

covering, with at least one second isolating layer, all portions of the memory cell array between the bitlines not covered by the wordlines;

removing the first isolating layer from the bitlines by a step in which also a topmost of the at least one second isolating layer is removed from the memory cell array at portions not covered by the wordlines; and

providing an electrical conductive material on exposed portions of the bitlines.

9. Pertaining to claim 6, An teaches the method according to claim S, which further comprises carrying out the step of removing the first isolating layer by time-controlled etching of the first isolating layer selectively with respect to the wordlines.

10. Pertaining to claim 7, An teaches the method according to claim 1, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing an isolating material onto the memory cell array;

coating a photoresist material and lithographically defining contact holes in the photoresist material;

etching the isolating material to create the contact holes; and

depositing the electrical conductive material to fill the contact holes with the electrical conductive material.

11. Pertaining to claim 8, An teaches the method according to claim 5, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing an isolating material onto the memory cell array;

coating a photoresist material and lithographically defining contact holes in the photoresist material;

etching the isolating material to create the contact holes; and

depositing the electrical conductive material to fill the contact holes with the electrical conductive material.

12. Pertaining to claim 9, An teaches the method according to claim 1, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

13. Pertaining to claim 10, An teaches the method according to claim 2, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

14. Pertaining to claim 11, An teaches the method according to claim 3, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

15. Pertaining to claim 12, An teaches the method according to claim 9, which further comprises carrying out the step of removing the electrical conductive material from the areas between the bitlines by:

coating a photoresist material on the electrical conductive material and lithographically defining regions where the electrical conductive material is to be removed using a mask having a stripe pattern; and

removing the electrical conductive material in the exposed regions.

16. Pertaining to claim 13, An teaches the method according to claim 5, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

17. Pertaining to claim 14, An teaches the method according to claim 6, which further comprises carrying out the step of providing the electrical conductive material on the exposed portions of the bitlines by:

depositing the electrical conductive material onto the memory cell array;

removing the electrical conductive material from areas between the bitlines; and

depositing an isolating material in the areas between the bitlines.

18. Pertaining to claim 15, An teaches the method according to claim 13, which further comprises carrying out the step of removing the electrical conductive material from the areas between the bitlines by:

coating a photoresist material on the electrical conductive material and lithographically defining regions where the electrical conductive material is to be removed using a mask having a stripe pattern; and

removing the electrical conductive material in the exposed regions.

19. Pertaining to claim 16, An teaches to teach the method according to claim 15, which further comprises carrying out the step of removing the first isolating layer from the bitlines to expose the substrate at the portions between the bitlines not covered by the wordlines, and performing the step of etching the electrical conductive material as an over-etching step to remove part of the substrate under the electrical conductive material.

20. Pertaining to claim 19, An teaches the method according to claim 1, which further comprises carrying out the electrical conductive material providing step by providing doped polysilicon on exposed portions of the bitlines.

21. Pertaining to claim 20, An teaches the method according to claim 5, which further comprises carrying out the electrical conductive material providing step by providing doped polysilicon on exposed portions of the bitlines.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over An, U.S. Patent 5,624,862 in view of Azmanov, U.S. Patent 5,517,061.

An discloses a semiconductor process substantially as claimed.

24. Pertaining to claim 17, An fails to teach the method according to claim 9, which further comprises carrying out the depositing an isolating material depositing step by depositing, in the areas between the bitlines, a silicate glass doped with at least one of boron and phosphorous. However, Azmanov teaches a silicate glass doped with at least one of boron and phosphorous (BPSG), in view of Azmanov, it would have been obvious to incorporate the limitations of a BPSG into the An process because the BPSG layer furnishes insulation between the polysilicon gate and subsequently formed overlying metal layers (column 9, lines 60-63).

25. Pertaining to claim 18, An fails to teach the method according to claim 13, which further comprises carrying out the depositing an isolating material depositing step by depositing, in the areas between the bitlines, a silicate glass doped with at least one of boron and phosphorous. However, Azmanov teaches a silicate glass doped with at least one of boron and phosphorous (BPSG), in view of Azmanov, it would have been obvious to incorporate the limitations of a BPSG into the An process because the BPSG layer furnishes insulation between the polysilicon gate and subsequently formed overlying metal layers (column 9, lines 60-63).

26. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over An, U.S. Patent 5,624,862 in view of Camerlenghi et al., U.S. Patent 6,124,169.

An teaches a semiconductor process substantially as claimed.

27. Pertaining to claim 21, An teaches a method of fabricating a nitride read only memory chip, which comprises:

providing a memory cell array with memory cells, bitlines, and wordlines, each of the memory cells having a metal-insulator-semiconductor field effect transistor with disposing the

bitlines in a first direction and the wordlines in a second direction perpendicular to the first direction and above the bitlines;

disposing the memory cells at points at which the bitlines and the wordlines cross one another and at which the bitlines are covered by an isolating layer;

providing a peripheral portion having logic components;

providing an electrical contact between the bitlines and metal lines to be formed in a following step by forming bitline contacts by:

removing the isolating layer from the bitlines at portions not covered by the wordlines with areas between the bitlines remaining unaffected; and

providing an electrical conductive material on exposed portions of the bitlines; and

disposing the metal lines in the first direction above the bitlines. However, An fails to teach the insulator being an oxide-nitride-oxide multi-layer stack for storing at least one injected electron. Camerlenghi teaches the insulator being an oxide-nitride-oxide multi-layer stack for storing at lest one injected electron (column 5, line 44). In view of Camerlenghi, it would have been obvious to one of ordinary skill in the art to incorporate the ONO stack of Camerlenghi into the An semiconductor process because by applying appropriate voltages to the cell terminals it is possible to change a quantity of charge present in the floating gate (column 1, lines 38-40).

28. Pertaining to claim 22, An teaches a method of fabricating a nitride read only memory chip, which comprises:

providing a memory cell array with memory cells, bitlines, and wordlines, each of the memory cells having a metal-insulator-semiconductor field effect transistor;

disposing the bitlines in a first direction on a substrate and the wordlines in a second direction perpendicular to the first direction and above the bitlines on the substrate;

disposing the memory cells at points at which the bitlines and the wordlines cross one another and at which the bitlines are covered by a first isolating layer;

providing a peripheral portion having logic components;

providing an electrical contact between the bitlines and metal lines to be formed in a following step by forming bitline contacts by:

covering, with at least one second isolating layer, all portions of the memory cell array between the bitlines not covered by the wordlines;

removing the first isolating layer from the bitlines by a step in which also a topmost of the at least one second isolating layer is removed from the memory cell array at portions not covered by the wordlines; and

providing an electrical conductive material on exposed portions of the bitlines; and

disposing the metal lines in the first direction above the bitlines. However, An fails to teach the insulator being an oxide-nitride-oxide multi-layer stack for storing at least one injected electron. Camerlenghi teaches the insulator being an oxide-nitride-oxide multi-layer stack for storing at lest one injected electron (column 5, line 44). In view of Camerlenghi, it would have been obvious to one of ordinary skill in the art to incorporate the ONO stack of Camerlenghi into the An semiconductor process because by applying appropriate voltages to the cell terminals it is possible to change a quantity of charge present in the floating gate (column 1, lines 38-40).

29. Pertaining to claim 23, An in view of Camerlenghi teaches a memory cell array having bitline contacts produced by the method according to claim 1.

30. Pertaining to claim 24, An in view of Camerlenghi teaches a memory cell array having bitline contacts produced by the method according to claim 5.

31. Pertaining to claim 25, An in view of Camerlenghi teaches a nitride read only memory chip fabricated by the method of claim 21.

32. Pertaining to claim 26, An in view of Camerlenghi teaches a nitride read only memory chip fabricated by the method of claim 22.

Conclusion

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

34. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

35. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC